parallel lines extending in the first direction and lying in a third plane above the first and second planes such that each of the third level lines is coplanar with a respective one of said line pairs; and

a second dielectric layer disposed between the second and third levels of conductive lines,

so that the third level of lines vertically extends the array of at least four parallel capacitor plates.

6. (Amended) The capacitor of claim 1, wherein the first and the at least second multiple levels of electrically conductive parallel lines comprise a plurality of electrically conductive parallel lines arranged in vertical plates, and the dielectric layer comprises a plurality of dielectric layers, each of the layers disposed between opposing levels of conductive lines.

A marked up copy of claims 1, 5, and 6, showing all changes made relative to the previous version of the claim, accompanies this paper on a separate sheet or sheets per 37 CFR § 1.121(c)(1)(ii).

REMARKS

Claims 1-11 are pending in the application. Claims 1, 5, and 6 are amended.

The Office action objects to the Drawing of the invention under 37 CFR 1.84(p)(4), stating that reference characters "27" and

"30" have both been used to designate conductive via and dielectric layer. Applicants respectfully submit that reference character "27" has an arrow that points to the entire second dielectric layer 27, consistent with 37 CFR 1.84(r)(1). Conversely, the reference characters "30" have line segments that extend directly to electrically conductive vias 30 that are formed in the dielectric layer 27, consistent with 37 CFR 1.84(q). Accordingly, withdrawal of the objection to the Drawing of the invention under 37 CFR 1.84(p)(4) is respectfully requested.

The Office action objects to the Drawing of the invention under 37 CFR 1.84(a), stating that Fig. 2B "clearly depicts dielectric layer comprising vacuum." Applicants respectfully submit that there is no symbol or other indication in the drawing signifying vacuum, and no mention of vacuum in the specification. The specification teaches a first dielectric layer 26, and the drawing correctly points to the space in which it is located. Since the specification correctly states that this is a dielectric layer, there is no conflict. Accordingly, withdrawal of the objection to the Drawing of the invention under 37 CFR 1.84(a) is respectfully requested.

The Office action rejects to claims 1-11 under 35 U.S.C. § 112, first paragraph and 35 U.S.C. § 112, second paragraph. Claims 1, 5, and 6 are amended to comply with 35 U.S.C. § 112. Accordingly, withdrawal of the rejections under 35 U.S.C. § 112,

first paragraph and 35 U.S.C. § 112, second paragraph is respectfully requested.

The Office action rejects claims 1-3 and 5-7 under 35 U.S.C. § 102(b) over U.S. Patent No. 5,583,359 to Ng et al. Applicants respectfully traverse this rejection. Claims 1-3 and 5-7 are patentable under 35 U.S.C. § 102(b) at least because Ng et al. do not teach or suggest that the first level line and the second level line of each of the at least four line pairs is connected by at least a respective one of the plurality of vias, thereby forming an array of at least four parallel capacitor plates, as recited in independent claim 1. Conversely, Ng et al. teach vias only connecting lines at opposing ends of the horizontal plates, which is equivalent to forming only two parallel capacitor plates. Claims 2, 3, and 5-7 depend, either directly or indirectly, from claim 1. Accordingly, withdrawal of the 35 U.S.C. § 102(b) rejection of claims 1-3 and 5-7 is respectfully requested.

The Office action rejects claims 1-11 under 35 U.S.C. § 103(a) over Ng et al. Applicants respectfully traverse this rejection. Claims 1-3 and 5-7 are patentable under 35 U.S.C. § 103(a) for the same reasons explained above, and claim 6 is patentable over Ng et al. at least because it depends from claim 1, which is patentable as explained above. Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection of claims 1-11 is respectfully requested.

In view of the foregoing, applicants respectfully request that the Examiner withdraw the rejections of record, allow all the pending claims, and find the present application to be in condition for allowance. If any points remain in issue that the Examiner feels may best be resolved through a personal or telephonic interview, he is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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MARKED-UP AMENDED CLAIM(S)

1. (Amended) A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction and lying in a first plane;

at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying in a second plane above the first plane,

each of the second level lines being disposed over a respective one of ~~the lines in~~ the first level lines, such that the lines of the first and second levels ~~being~~ are arranged in ~~vertical rows~~ a series of at least four coplanar line pairs, each line pair comprising one of the first level lines and a respective one of the second level lines;

a dielectric layer disposed between the first and second levels of conductive lines;

a plurality of vias arranged such that the first level line and the second level line of each of the at least four line pairs is connected by at least a respective one of the plurality of vias ~~via connecting the lines in each of the rows~~, thereby forming ~~a parallel~~ an array of at least four ~~vertical~~ parallel capacitor plates; and

electrically opposing nodes forming the terminals of the capacitor, the ~~parallel~~ array of ~~vertical~~ parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

5. (Amended) The capacitor of claim 1, further comprising:

at least a third level of at least four electrically conductive parallel lines extending in the first direction and lying in a third plane above the first and second planes ~~disposed~~

~~over the second level lines in manner which extends the rows vertically~~ such that each of the third level lines is coplanar with a respective one of said line pairs; and

a second dielectric layer disposed between the second and third levels of conductive lines,~~; and~~

~~at least one via connecting the second and third level lines in each of the rows~~ so that the third level of lines vertically extends the ~~parallel~~ array of at least four ~~vertical~~ parallel capacitor plates.

6. (Amended) The capacitor of claim 1, wherein the first and the at least second multiple levels of electrically conductive parallel lines comprise a plurality of electrically conductive parallel lines arranged in vertical ~~rows~~ plates, and the dielectric layer comprises a plurality of dielectric layers, each of the layers disposed between opposing levels of conductive lines.